This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) An apparatus comprising:

a plurality of logic modules, wherein at least two logic modules are configured to selectively process image related data according to different image processing algorithms;

a plurality of bus interfaces, each bus interface being operatively coupled to a corresponding logic module; and

a plurality of buses including at least a memory bus, a first support bus and a second support bus, wherein each bus interface is selectively programmably configurable to ~~configured to selectively~~ operatively couple the corresponding logic module to at least a programmably selected one of the first support bus and the second support bus in response to at least one programming control input to selectively route at least a portion of the image related data between the at least two logic modules for processing in accordance with a programmable data processing order.

2. (cancelled)

3. (previously presented) The apparatus as recited in Claim 1, further comprising a memory bus interface operatively coupled to the memory bus.

4. (original) The apparatus as recited in Claim 3, wherein the memory bus interface is further configured as a memory controller and configurable for use with memory.

5. (original) The apparatus as recited in Claim 4, further comprising memory operatively coupled to the memory bus interface.

6. (original) The apparatus as recited in Claim 5, wherein the memory bus is configured to selectively route the image related data between the memory and at least one of the plurality of logic modules via the bus interface associated with the at least one logic module and the memory bus interface.

7. (cancelled)

8. (cancelled)

9. (previously presented) The apparatus as recited in Claim 1, wherein at least two of the plurality of logic modules are configured to share information by sending and receiving one or more messages via at least one of the plurality of buses.

10. (original) The apparatus as recited in Claim 9, wherein the message includes at least one identifier selected from a group of identifiers comprising a destination identifier, a source identifier, and a bus identifier.

11. (original) The apparatus as recited in Claim 9, wherein the message includes a data field capable of carrying the image related data.

12. (original) The apparatus as recited in Claim 11, wherein the image related data carried in the data field of the message includes at least one form of data selected from a group of data comprising image data, index data, and address data.

13. (original) The apparatus as recited in Claim 1, wherein at least one of the plurality of logic modules is configured to selectively process at least a portion of the image related data according to an image processing algorithm selected from a group of image processing algorithms comprising a half-toning algorithm, a filtering algorithm, a convolution algorithm, an integrating algorithm, a template matching algorithm, a thresholding process algorithm, a matrix operating algorithm, a decoder algorithm, a decompression algorithm, a coder algorithm, and a compression algorithm.

14. (original) The apparatus as recited in Claim 1, wherein the data processing order is associated with an image processing pipeline.

15. (cancelled)

16. (currently amended) An apparatus comprising:

a plurality of logic modules, each logic module being configured to selectively process image related data according to a different image processing algorithm;

a plurality of bus interfaces, each bus interface being operatively coupled to a corresponding logic module; and

a plurality of buses, including at least a memory bus, a first support bus and a second support bus, operatively coupled to the plurality of bus interfaces, and wherein each of the plurality of bus interfaces is selectively programmably configurable to ~~selectively~~ route image related data through either the first support bus or the second support bus to the corresponding logic module for processing in accordance with a programmable data processing order.

17. (original) The apparatus as recited in Claim 16, wherein the image related data includes at least one form of data selected from a group of data comprising image data, index data, and address data.

18. (original) The apparatus as recited in Claim 16, wherein at least one of the plurality of logic modules is configured to selectively process at least a portion of the image related data according to an image processing algorithm selected from a group of image processing algorithms comprising a half-toning algorithm, a filtering algorithm, a convolution algorithm, an integrating algorithm, a template matching algorithm, a thresholding process algorithm, a matrix operating algorithm, a decoder algorithm, a decompression algorithm, a coder algorithm, and a compression algorithm.

19. (original) The apparatus as recited in Claim 17, wherein the programmable data processing order causes an image processing pipeline to be formed using at least a portion of the plurality of logic modules.

20. (currently amended) An image processing device comprising:

a plurality of buses, including at least a memory bus, a first support bus and a second support bus;

memory suitable for storing image related data;

a memory bus interface coupled to the memory bus and the memory and configured to provide access to the memory via the memory bus;

a plurality of logic modules, each logic module being configured to process image related data according to a different image processing algorithm; and

a plurality of bus interfaces, each bus interface being coupled to a corresponding logic module, the first support bus, the second support bus and the memory bus, and selectively programmably configurable to ~~selectively~~ route the image related data through the first support bus or the second support bus to the plurality of logic modules for processing in accordance with a programmable data processing order.

21. (original) The image processing device as recited in Claim 20, wherein the image related data includes at least one form of data selected from a group of data comprising image data, index data, and address data.

22. (original) The image processing device as recited in Claim 20, wherein at least one of the plurality of logic modules is configured to selectively process at least a portion of the image related data according to an image processing algorithm selected from a group of image processing algorithms comprising a half-toning algorithm, a filtering algorithm, a

convolution algorithm, an integrating algorithm, a template matching algorithm, a thresholding process algorithm, a matrix operating algorithm, a decoder algorithm, a decompression algorithm, a coder algorithm, and a compression algorithm.

23. (original) The apparatus as recited in Claim 20, wherein the data processing order causes an image processing pipeline to be formed using at least a portion of the plurality of logic modules.

24. (original) The apparatus as recited in Claim 20, wherein the data processing order is established via control inputs to the plurality of bus interfaces.

25. (original) The image processing device as recited in Claim 20, wherein the image processing device is selected from a group of image processing devices comprising a color printing device, monochrome printing device, an image scanning device, a facsimile device, an image copying device, an image reproduction device, and image displaying device, an image generating device, an image capturing device a still camera device, and a video camera device.